# Faculty Profile on University Website

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| **Title** | Dr. | **First Name** | YOGRAJ SINGH | **Last Name** | DAKSH | **Photograph** |
| **Designation** | | Professor | | | |  |
| **Department** | | Electronics & Instrumentation Engineering | | | | |
| **Address** | **Campus** | Faculty of Engineering & Technology<br>M.J.P. Rohilkhand University, Bareilly-243006, India | | | | |
| | **Residence** | 13/A, Amber, Supercity, Bareilly-243006 | | | | |
| **Mobile No.** | | 7906553046 | | | | |
| **Email ID** | | University Domain | | | | ysdaksh.ei@mjpru.ac.in |
| | | Personal | | | | yograj.siet@gmail.com |
| **Professional Networking ID, i.e. LinkedIn, Twitter etc.** | | LinkedIn: https://www.linkedin.com/in/dr-yograj-singh-97b49116/ | | | | |

**Educational Qualifications:**

| Course/Degree | Institution | Year | Details/Thesis Topic/Subjects |
|---|---|---|---|
| Ph. D. (Electronics Engineering) | Shobhit University, Meerut (Deemed University U/S 3 of UGC Act 1956) | 2016 | Crosstalk and Propagation Delay Analysis in Modern VLSI Interconnects |
| M. Tech. (Instrumentation Engineering) | Regional Engineering College (now NIT, Kurukshetra) Kurukshetra | 2001 | A Study of Interconnect Parasitics in VLSI-chips (Dept of ECE, IIT Roorkee) |
| M. Phil (Instrumentation) | University of Roorkee (now IIT Roorkee), Roorkee | 1999 | A Structural Tilt Measurement System (CBRI, Roorkee) |
| M.Sc. (Physics) | Rohilkhand University, Bareilly | 1996 | Specialization in Electronics |

**Career Profile:**

| Organization / Institution | Designation | Duration | Nature of Duties |
|---|---|---|---|
| M.J.P. Rohilkhand University, Bareilly | Professor | 17 April, 2016 to till date | Academic, Administrative & Research |
| M.J.P. Rohilkhand University, Bareilly | Associate Professor | 29 September, 2011 to 16 April, 2016 | Academic, Administrative & Research |
| M.J.P. Rohilkhand University, Bareilly | Reader | 29 September, 2008 to 28 September, 2011 | Academic & Research |
| Shobhit University, Meerut (Deemed University U/S 3 of UGC Act 1956) | Assistant Professor | 01 August, 2007 to 28 September, 2008 | Academic & Research |
| Shobhit Institute of Engineering & Technology, Meerut | Lecturer /Sr. Lecturer | 05 August, 2005 to 31 July, 2007 | Academic |
| Teerthankar Mahaveer Institute of Management & Technology, Moradabad | Lecturer | 21 February, 2002 to 04 August, 2005 | Academic |

**Research Interests / Specialization**

- Modeling of Hybrid VLSI Interconnects
- Modeling and Simulation of CNT/GNR based VLSI Interconnects
- Modeling and Simulation of Junction-less FETs
- Instrumentation Systems and Measurement Techniques

**Research Experience:** 18 years
**Teaching Experience:** 24 years

**Academic/Administrative Positions/Assignments Held:**

- Convener, Board of Study, Department of Electronics & Instrumentation Engineering from 2013 to 2017.
- Observer, B.Ed. Entrance Examination from 2017 to 2018.
- Observer, M.Sc. Entrance Examination since 2019
- Head, Department of Electronics & Instrumentation Engineering from July 2015 to July 2018.
- Member, Academic Council Since June 2023.
- Department Coordinator, NAAC Accreditation Committee from 2015-2016 and 2020-2023.
- Nodal Officer, Anti-Narcotics Taks Force under Nasha Mukt Bharat Abhiyaan since June 2023.
- Nodal Officer, Moderation Committee, M.J.P. Rohilkhand University, Bareilly since Feb 2024.
- Coordinator, FET Examination from July 2025 to August 2026.

**No of Research Scholars:** 01 (Ongoing)

| ***Name of Programme*** | ***Awarded*** | ***Under Supervision*** |
|---|---|---|
| Ph.D. | Ongoing | Myself |

| **Researcher/ Expert ID** | **Scopus** | **Orchid** | **Publons** | **Vidwan** | **Google Scholar** |
|---|---|---|---|---|---|
| | 36805538500 | 0000-0002V-5004-7283 | AAZ-5057-2020 | 165546 | EQU0KHIAAAAJ |

**Total Teaching Experience (Subjects/Courses Taught):**

*At B.Tech. Level:*
Solid State Electronic Devices; Linear Integrated Circuits; VLSI Technology; VLSI Deign; Semiconductor Fabrication Technology, Fundamental of Nanoelectronics, Integrated Circuit Technology and Design, Industrial Instrumentation, Transducers Sensors and Display Devices, Biomedical Instrumentation, Digital Electronics, Control System, Electronic Engineering Materials
*At M.Tech. Level and Ph.D. Course work:* Digital VLSI Design

**Scholarship:**

- Qualified Graduate Aptitude Test in Engineering (GATE-1999) with *AIR 170* and got scholarship by MHRD from 1999 to 2001 during M.Tech. Program.

**Research Projects Completed:**

| **Year** | **Type of Project** | **Title of Project** | **Funding Agency** | **Amount** | **Status of the Project** | **Duration** | |
|---|---|---|---|---|---|---|---|
| | | | | | | **From** | **Till** |
| 2011 | Minor Research Project | Circuit Modeling and Performance Analysis of SWCNTs for the Application of future VLSI Interconnects. | UGC, New Delhi | 0.70 Lakh | Completed | Feb., 2011 | Jan., 2013 |
| 2019 | Minor Research Project | Analysis of Intercalated Doped ML-GNR Interconnects. | NPIU, MHRD, New Delhi (Seed Grant under TEQIP-III) | 2.0 Lakh | Completed | June, 2019 | June, 2021 |

**Publication in Referred Journals:**

| **Year of Publication** | **Title** | **Name of Journal** | **ISSN No.** | **Citations** | **Impact Factor** |
|---|---|---|---|---|---|
| **2010** | Performance comparison of carbon nanotubes, nickel silicide nanowire and | Journal of Engineering, Design and Technology, Emerald, Vol. 8, No. 3, pp. 334-353, 2010. | 1726-0531 | 07 | 0.76 |

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| | copper VLSI interconnects: perspectives and challenges ahead. | | | | |
| **2013** | Analysis of Propagation Delay and Power with Variation in Driver Size and Number of Shells in Multi Walled Carbon Nanotube Interconnects. | Journal of Engineering, Design and Technology, Emerald, Vol. 11, No. 1, pp. 19-33, 2013. | 1726-0531 | 09 | 0.76 |
| **2015** | FDTD Technique based crosstalk analysis of bundled SWCNT interconnects. | Journal of Semiconductors, IOP, Vol. 36, No. 5, pp. 055002-1-55002-9, 2015. | 1674-4926 | 21 | 1.18 |
| **2018** | Delay and Power Analysis of Bundled SWCNT Interconnects with variation in driver size. | International Journal of Research in Electronics and Computer Engineering, Vol.6, No.4, pp. 860-866, 2018 | 2393-9028 | – | – |
| **2020** | Subthreshold Modeling of Graded Channel Double Gate Junctionless FETs | Silicon Journal, Springer, Vol. 13, Issue: 04 (April 2021), pp. 1231-1238, 2020 Published online: 25 May, 2020 | 1876-9918 | 07 | 3.4 |
| **2021** | Self-heating and Negative Differential Conductance Improvement by Substrate Bias Voltage in Tri-gate Junctionless Transistor | Silicon Journal, Springer Published on 04 March, 2021 | 1876-9918 | 02 | 3.4 |

**Publications in Conferences:**

**(1)** **Yograj Singh Duksh**, Brajesh Kumar Kaushik, Sankar Sarkar and Rajendra Prasad Agarwal, "Effect of Driver Size and Number of Shells on Propagation Delay in MWCNT Interconnects", in *IEEE International Conference on Devices & Communications (ICDeCom-2011),* Ranchi, Jharkhand, February 24 -25, 2011.

**(2)** Lalita Gangwar, and **Yograj Singh Duksh**, "Hybrid Interconnects as Future VLSI Interconnects-A Review", in the International Conference in Smart and Sustainable Engineering (ICISSE-2026) organized by Electrical Engineering Department, Teerthankar Mahaveer University, College of Engineering, Moradabad on 15th May, 2026.

**(3)** Lalita Gangwar, Mukesh Kumar Sone, Anil Kumar Singh and **Yograj Singh Duksh**, "A Study of Cu-GNR Interconnects in Microstrip Antenna Feeding Networks", in the International Conference in Smart and Sustainable Engineering (ICISSE-2026) organized by Electrical Engineering Department, Teerthankar Mahaveer University, College of Engineering, Moradabad on 15th May, 2026.

**Books/Book Chapter Published:** No, please.

**Refresher Course/Short Term Course/Faculty Development Program/Conferences/Workshops Attended:**

- Refresher Courses Attended: 02
- Faculty Development Programs Attended: 05 [02 (Two weeks) + 03 (One week)]
- Short Term Courses Attended: 05 [01 (Two weeks) + 04 (One week)]
- Summer School Attended: 03 [01 (Two weeks) + 02 (One week)
- Virtual Summit Attended: 01 (One week)
- Workshop Attended: 06 [03 (Two days) + 03 (One day)]
- Mini-Colloquium Attended: 01 (One day)
- Conferences Attended: 02

**Invited as Examiner/Expert:**

- External Examiner: To conduct the viva-voce examination of M.Tech. dissertation at Department of Electronics & Communication Engineering, College of Technology, G.B. Pant University of Agriculture and Technology, Pantnagar, Uttarakhand from 2018 to 2019.
- External Examiner: To conduct the end-semester lab examination of B.Tech. at Department of Electronics & Communication Engineering, Faculty of Engineering and Technology, Gurukul Kangri University from 2010 to 2018, Haridwar, Uttarakhand.
- End-semester question paper setter at B.Tech. and M.Tech. level of M.J.P. Rohilkhand University, Campus, Bareilly since 2008.
- End-semester question paper setter at B.Tech. level of Gurukul Kangri University, Haridwar, Uttarakhand from 2016 to 2018.
- End-semester question paper setter at B.Tech. level of College of Technology, Teerthanker Mahaveer University, Moradabad from 2015 to 2018

**Memberships of Academic/Professional Bodies:**

- Fellow- Institution of Electronics and Telecommunication Engineers (IETE), New Delhi: F-501674
- Fellow- The Institution of Engineers India (IEI), Kolkata : F-1271020
- Life Member- The Indian Society of Technical Education (ISTE) : LM-69993

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| ▪ Life Member- Instrument Society of India (ISOI), Bangaluru : LM-1935<br>▪ Senior Member - Institute of Electrical and Electronics Engineers (IEEE), USA : SM-97206502<br>▪ Annual Member-Indian Physics Association (IPA) : AM/35 |
| **Any Other Details:** |
| **Reviewers of the following Journals:**<br>(i) Microelectronics Journal<br>(ii) Micro and Nano Letters<br>(iii) Arabian Journal for Science and Engineering |

Prof. (Dr.) Yograj S. Daksh
Name & Signature of Faculty Member